IN THE ABSTRACT

Please amend the abstract as follows:

~~The invention proposes a~~ A ~~phase detector for a~~ phased-locked loop phase detector for digital input signals in which digital summed value for a particular number of bits is equal to zero. ~~In this context, it relates to an improvement in the phase detector which can be used in a digital PLL circuit. The intention consists in a sampled~~ Sampled and digitized data ~~signal being supplied to the phase detector as an input signal. This~~ comprising a delay stage for delaying the data signal ~~is delayed~~ by a one or more sampling clock ~~signal~~ period ~~in a delay stage~~ is supplied to the phase detector as an input signal. The delayed data signal and the undelayed data signal are then supplied to a subtraction stage. The difference between the two input values is formed in this subtraction stage. The processing stage assigns ~~differential value determined is then analyzsed in a processing stage and~~ one of a plurality of possible values ~~is assigned~~ to ~~it~~ the respective differential value. ~~This is done on the basis of the value range in which the differential value is situated. The assigned value is then passed on as an output value to a filter/control stage, at whose output a phase error can then be tapped off. The solution described can be integrated very easily on a chip and affords a very advantageous response for the PLL control.~~ The full differential value range is subdivided in a number of sub-ranges corresponding to the plurality of possible values. All differential values in one sub-range are assigned the same output value. The output of the subtraction stage is supplied to a filter/control stage.